AMENDMENT TO THE DRAWINGS

Please replace the originally filed drawing sheets containing Figs. 10 and 11 with the attached Replacement Sheet containing Figs. 10 and 1111. Fig. 11 replacement sheet has now been labeled 'Prior Art.' Applicants state that no new matter has been added either by deletion and/or addition. Therefore, acceptance of the two replacement sheets of drawings containing Figs. 10 and 11 is respectfully requested.

REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This amendment is in response to the Office Action dated March 12, 2009.

By the present amendment, the drawings and claims have been amended to respond to the various objections and rejections as set forth in the Office Action.

Beginning with page 2 of the Office Action, reconsideration and removal of the objection to the drawings set forth therein is respectfully requested. With regard to the objection concerning claim 16, this claim has been canceled, without prejudice. With regard to the objection concerning claim 27, it is respectfully submitted that the subject matter of this claim can be found in Fig. 8 as well as the discussion in paragraph [0064] and [0065] of the published U.S. Application Serial No. 2002/0171138 for the present application. For example, paragraph [0064] clearly states:

> "The embodiment shown in Fig. 8 is substantially the same as that shown in Fig. 5 but is constructed such that thermal vias 4 are not arranged only below emitter electrodes disposed nearest two ends (chip ends in the Fig.) of the semiconductor substrate 1."

Similarly, in paragraph [0065] it is stated:

> "thermal vias 4 are arranged immediately below those ones disposed centrally of emitters thus arranged, but not arranged immediately below the emitters in the peripheral portions."

It is noted that Fig. 2(c) also illustrates an arrangement with the rows of emitter electrodes 7, the emitter wirings 10 and the thermal vias 4 in which it is obvious that the thermal vias 4 are not arranged immediately below the emitter electrodes 7 on both

ends in the sectional view. For these reasons, reconsideration and removal of the objection to the drawing regarding Fig. 27 is respectfully requested.

With regard to Fig. 11, it is noted that this has been labeled Prior Art by this Amendment.

With regard to the objection to the drawings set forth on page 3 of the Office Action, the numeral 14 has been deleted from Fig. 10 by this Amendment. Concerning the objection to the drawing concerning the location of the reference numeral 10 in Fig. 11, it is respectfully submitted that this actually shows the proper location for the emitter wirings 10 extending over the emitter electrodes 7. However, Fig. 10 has been amended to correct the labeling to show the emitter electrodes 7 (which had previously been mislabeled with the numeral 10), and it appears that this amendment to Fig. 10 should clear up any confusion concerning Fig. 11. In any event, reconsideration and removal of the objections to the drawings set forth on page 3 are also respectfully requested.

Reconsideration and removal of the 35 USC §112, first paragraph, rejections of claims 16 and its dependent claims set forth on page 4 is also respectfully requested. As noted above, these claims have been canceled without prejudice, thereby obviating the rejections.

With regard to the 35 USC §112 rejection of claim 27, set forth on page 5 of the Office Action, it is noted that claim 7 has been amended to clarify the relationship regarding the through holes of the multilayer wiring board with the emitter electrodes. It is further noted that Fig. 8 and paragraphs [0064] and [0065] clearly support the claim limitations for the reasons discussed above with regard to the objection to the drawings.

Therefore, reconsideration and removal of the 35 USC §112, first paragraph, rejection of claim 27 set forth on page 5 is also respectfully requested.

Reconsideration and removal of the 35 USC §112, first paragraph, rejection of claims 26, 48, 49 and 54 as failing to comply with the enablement requirement is also respectfully requested. Regarding this, the language of the parent claim 26 has been corrected so that the through holes of the multilayer wiring board are defined, rather than the previous erroneous language concerning the through holes of the semiconductor substrate. therefore, it is respectfully submitted that the amendment obviates this rejection, and its removal is respectfully requested.

Reconsideration and removal of the 35 USC §112, second paragraph, rejection of various claims set forth beginning on page 6 of the Office Action is also respectfully requested. By the present amendment, these claims have been revised to correct the informalities noted in the Office Action. Accordingly, reconsideration and removal of these rejections is earnestly solicited. Also, examination of all claims on the merits in light of the clarified language is respectfully requested, noting the indication beginning on page 7 of the Office Action that the claim 26 and its dependent claims have not been examined over prior art.

Reconsideration and allowance of claims 14-20, 31, 32, 50 and 52 over the 35 USC §102(e) rejection based on Hayasaka (USP 6,809,421), reconsideration and removal of the 35 USC §102(a) rejection of claims 21 and 22 over the applicants admitted prior art (see page 19 of the Office Action, noting that, with regard to claims 16, 18, 19, 34 and 51, this rejection has been obviated by the cancellation of these claims) and reconsideration and removal of the 35 USC §103(a) rejection of claims 14-

23, 25, 27-32, 34-47, and 50-53 over the combination of the applicants admitted prior art in view of Hayasaka is respectfully requested. With regard to this, it is respectfully submitted that the newly cited Hayasaka reference, although of general interest, completely fails to teach or suggest the features defined in the claims that is applied against it. Specifically, Hayasaka is of general interest for an arrangement which shows a plurality of semiconductor substrates 2 stacked upon one another with inner layer insulating films therebetween in which through holes with plugs (4) are provided in each of the substrates (2) so that the semiconductor substrates can be stacked on one another using solder bumps 8 contacting the respective through hole plugs 4. Regarding this, it is noted that Hayasaka is not concerned with heat dissipation in the stacked chips, and, as such, has no disclosure regarding the claimed relationships of the thermal vias set forth in the present claims. Concerning heat dissipation, the only disclosure provided in Hayasaka is an illustration of a radiation fin 39 placed on a top surface of the uppermost chip in the stacked chip shown in Fig. 18. This has absolutely nothing to do with the claimed thermal via arrangements, and the relative locations of elements with regard to the thermal vias, defined in the present amended claims. With regard to this, it is noted that each of the independent claims has been amended to specifically define that the through holes in the multilayer wiring board forms a thermal via, by emphasizing the distinction over the newly cited Hayasaka reference. Incidentally, it is noted that this is clearly supported in the specification, which refers to these through holes in the multilayer wiring board as the "thermal vias 4."

In the Office Action, it is argued that the position of the plugs 4 for a chip 1b shown in Fig. 5 of Hayasaka overlaps with a solder bump 8 formed in the chip 1c in a

thicknesswise direction. However, the through plug 4 and the solder bump 8 in Hayasaka are bonded to one another, thereby simply forming a wiring between them. There is absolutely no corollary in Hayasaka for providing a through hole in a multilayer wiring board, which through hole forms a thermal via in the multilayer wiring board, in conjunction with the other claimed arrangements regarding relative relationships of elements to these thermal vias.

Although it is also argued in the Office Action that combining the structure of Hayasaka with the admitted prior art shown in Fig. 3 of the present application would render the present claims obvious, it is respectfully submitted since there is no discussion whatsoever concerning the use of the through holes 4 or the solder bumps 8 in Hayasaka for heat dissipation purposes, there is absolutely no motivation for the claimed combination. If heat is conducted between the through holes 4 and the solder bumps 8 in Hayasaka, the heat from the semiconductor substrate will be diffused in an in-plane direction and will then be conducted in the through plug and the solder bump in a cross-plane direction of the substrate. This would result in generated heat having to effectively be bent from the in-plane direction to the cross-plane direction, which is completely different than the arrangements provided in the present claims for conducting heat in a substrate in a cross-plane direction.

In any event, it is respectfully submitted that it represents complete hindsight, solely with benefit of the applicants invention, to propose modification of the admitted prior art using Hayasaka, which fails to provide any discussion concerning heat dissipation using its plugs 4 and the solder bumps 8. Hayasaka simply shows a stacking arrangement for electrical connections, and, as such, would not be something

one would ordinarily consider when looking at the admitted prior art of the present application. Therefore, reconsideration and removal of these grounds for rejection is respectfully requested.

With regard to independent claims 21 and 22, arguments are set forth on page 20 of the Office Action that through holes are distributed in the multilayer wiring board of the admitted prior art which will be inherently aligned in the manner defined by the present claims. It is respectfully submitted that there is no basis in the admitted prior art for this argument based upon inherency. Therefore, if the next Office Action continues with this rejection, it is respectfully requested that further detailed comments be provided concerning such alleged inherency. Otherwise, reconsideration and removal of the rejection is earnestly solicited.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 500.40530X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
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APPENDIX